Claims:

1.   A method comprising:

introducing a multi-cycle instruction including two or more sub-instructions into a pipeline;

writing a result generated in response to a sub-instruction in a speculative commit register; and

writing a value in the speculative commit register to an architectural register in response to the multi-cycle instruction committing.

2.   The method of claim 1, wherein writing the value to the to the architectural register comprises writing the value to a pointer register.

3.   The method of claim 1, wherein introducing the multi-cycle instruction into the pipeline comprises introducing a non-terminal sub-instruction and a terminal sub-instruction into the pipeline.

4.   The method of claim 3, wherein writing the value in response to the multi-cycle instruction committing comprises writing the value in response to the terminal sub-instruction committing.

5.   The method of claim 1, wherein writing the result comprises writing a frame pointer value.

6.   The method of claim 1, wherein writing the result comprises writing a stack pointer value.

7.   An article comprising a machine-readable medium which stores machine-executable instructions, the instructions causing a machine to:

introduce a multi-cycle instruction including two or more sub-instructions into a pipeline;

write a result generated in response to a sub-instruction in a speculative commit register; and

write a value in the speculative commit register to an architectural register in response to the multi-cycle instruction committing.

8.   The article of claim 7, wherein the architectural register comprises a pointer register.

9.   The article of claim 7, wherein the multi-cycle instruction comprises a non-terminal sub-instruction and a terminal sub-instruction.

10.   The article of claim 9, wherein the multi-cycle instruction commits when the terminal sub-instruction commits.

11.   The article of claim 7, wherein the architectural register comprises a frame pointer register.

12.   The article of claim 7, wherein the architectural register comprises a stack pointer register.

13.   A processor comprising:

a pipeline operative to execute a multi-cycle instruction including a terminal sub-instruction and a non-terminal sub-instruction;

an architectural register;

a speculative commit register operative to store results generated in response to the sub-instructions; and

a controller operative to control writing a result from the speculative commit register to the architectural register in response to the terminal sub-instruction committing.

14.   The processor of claim 13, further comprising a switching element comprising:

a first input data line coupled to the pipeline;

a second input data line coupled to the speculative commit register; and

an output data line coupled to the architectural register,

said switching element being operative to switch between the first input data line and the second input data line in response to control signals from the controller.

15. The processor of claim 13, wherein the switching element comprises a multiplexer.

16. The processor of claim 13, wherein the architectural register comprises a pointer register.

17. The processor of claim 13, wherein the architectural register comprises a stack pointer register.

18. The processor of claim 13, wherein the architectural register comprises a frame pointer register.

19. The processor of claim 13, wherein the multi-cycle instruction comprises an instruction operative to invoke a subroutine.

20. The processor of claim 13, wherein the multi-cycle instruction comprises an instruction operative to exit a subroutine.

21. The processor of claim 13, wherein the multi-cycle instruction comprises an instruction operative to push or pop two or more values from a stack in sequence.

22. A system comprising:

a static random address memory; and

a processor coupled to the static random access memory, said processor comprising:

a pipeline operative to execute a multi-cycle instruction including a terminal sub-instruction and a non-terminal sub-instruction;

an architectural register;

a speculative commit register operative to store results generated in response to the sub-instructions; and

a controller operative to control writing a result from the speculative commit register to the architectural register in response to the terminal sub-instruction committing.

23. The system of claim 22, wherein the architectural register comprises a frame pointer register.

24. The system of claim 22, wherein the architectural register comprises a stack pointer register.